中山大學資訊工程研究所碩士班考試
計算機結構試題

NOTE: The problems have been carefully checked before they are given to you. However, if there are questions which seem unclear or not well-defined to you, don't worry. You can make your own assumptions in such cases. Please state clearly in the answer sheet what's the problems and the assumptions you made. The grading is flexible.

1. Digital Logic Circuits (25%)

A sequential two's-complementer (S2C) that negates two's-complement numbers can be realized with a finite-state machine as will be described below. The S2C has a single data input line x and a single data output line z with two initial states S_0 and S_1. While in initial state S_0, the input $x=0$ will leave the circuit in S_0 and produce the output $z=0$. When x first becomes 1, a transition is made to S_1, and z becomes 1. Hence the two possible state transitions from S_0 are as follows:

$$S_0 \xrightarrow{0/0} S_0 \qquad S_0 \xrightarrow{1/1} S_1$$

Once in S_1, the S2C remains there indefinitely until the circuit is asynchronously reset. The possible transitions from S_1 are as follows:

$$S_1 \xrightarrow{0/1} S_1 \qquad S_1 \xrightarrow{1/0} S_1$$

1.1 (10%) Please derive the state table and the corresponding state diagram for the above S2C described above. Explain why the state diagram can implement the negation of a 2's complement number.

1.2 (15%) To realize the S2C circuit with a D flip-flop, we define a state variable f with $f=0$ and $f=1$ denoting S_0 and S_1 respectively. Please derive the excitation table containing relation among the primary input x, present state f, next state $f+$, secondary output D, and the primary output z. From the excitation table, design a logic diagram to realize the S2C which consists of a D flip-flop and some simple combinational logic gates.

2. Arithmetic Unit (25%)

Fast addition is a very desirable feature of an arithmetic circuit, and is usually one of the important factors determining how fast a microprocessor can run. The carry look-ahead addition (CLA) is the most widely used scheme for the design of a fast adder. Unlike the inexpensive but slow carry-ripple adder (CRA) that is composed of cascaded full adder cells, the CLA calculates the carry-out bits from two sets of auxiliary signals: the generate signal $g_i=x_iy_i$ and the propagate signal $p_i=x_i+y_i$ of the i-th. bits x_i and y_i.

2.1 (10%) Please express the Boolean functions for the carry-out bit c_i and the sum bit s_i in terms of p_i, g_i and c_{i-1}, the carry-out bit of the $(i-1)$-th. bit position.

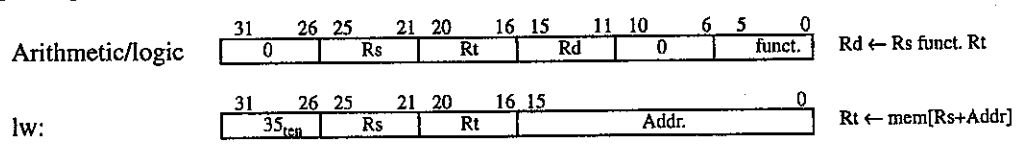
2.2 (15%) Recursively applying the Boolean function of c_i in 2.1, one can derive the carry-out bits of higher bit positions that depend on p_i, g_i, and initial carry-in bit c_0 only. Please design a 4-bit CLA computing $S=X+Y$ with $S=s_4s_3s_2s_1$, $X=x_4x_3x_2x_1$, and $Y=y_4y_3y_2y_1$ using the above concept. Write down the Boolean expressions for all the carry-out bits and the sum bits using p_i, g_i and c_0 only. Draw the logic gate realization of the 4-bit CLA. Based on the implementation of the 4-bit CLA, explain the reason why a CLA is faster than a CRA.

3. (30%) Pipeline Structure

Consider the five instructions in the following program. The instructions execute on a five-stage pipeline (in page 4). The five stages are: instruction fetch (IF), instruction decode and fetch operand (ID), instruction execution (EX), memory access (MEM) and register write back (WB), as shown in the following figure. Assume that each stage takes one cycle to complete its execution.

```
lw    $10, 20ten($1)        # $10 ← m[$1+20ten]
sub   $11, $2, $3           # $11 ← $2 - $3
and   $12, $4, $5           # $12 ← $4 ∧ $5
or    $13, $6, $7           # $13 ← $6 ∨ $7
add   $14, $8, $9           # $14 ← $8 + $9
```

The instruction formats are as the following. For the arithmetic/logic instructions, the *funct.* field is 30_{ten} for add, 32_{ten} for sub, 34_{ten} for and, 35_{ten} for or, respectively. Note that Rd, Rs, and Rt are register specifiers. The decimal representation of the register specifier is 17_{ten} for $1, 18_{ten} for $2, *etc.*



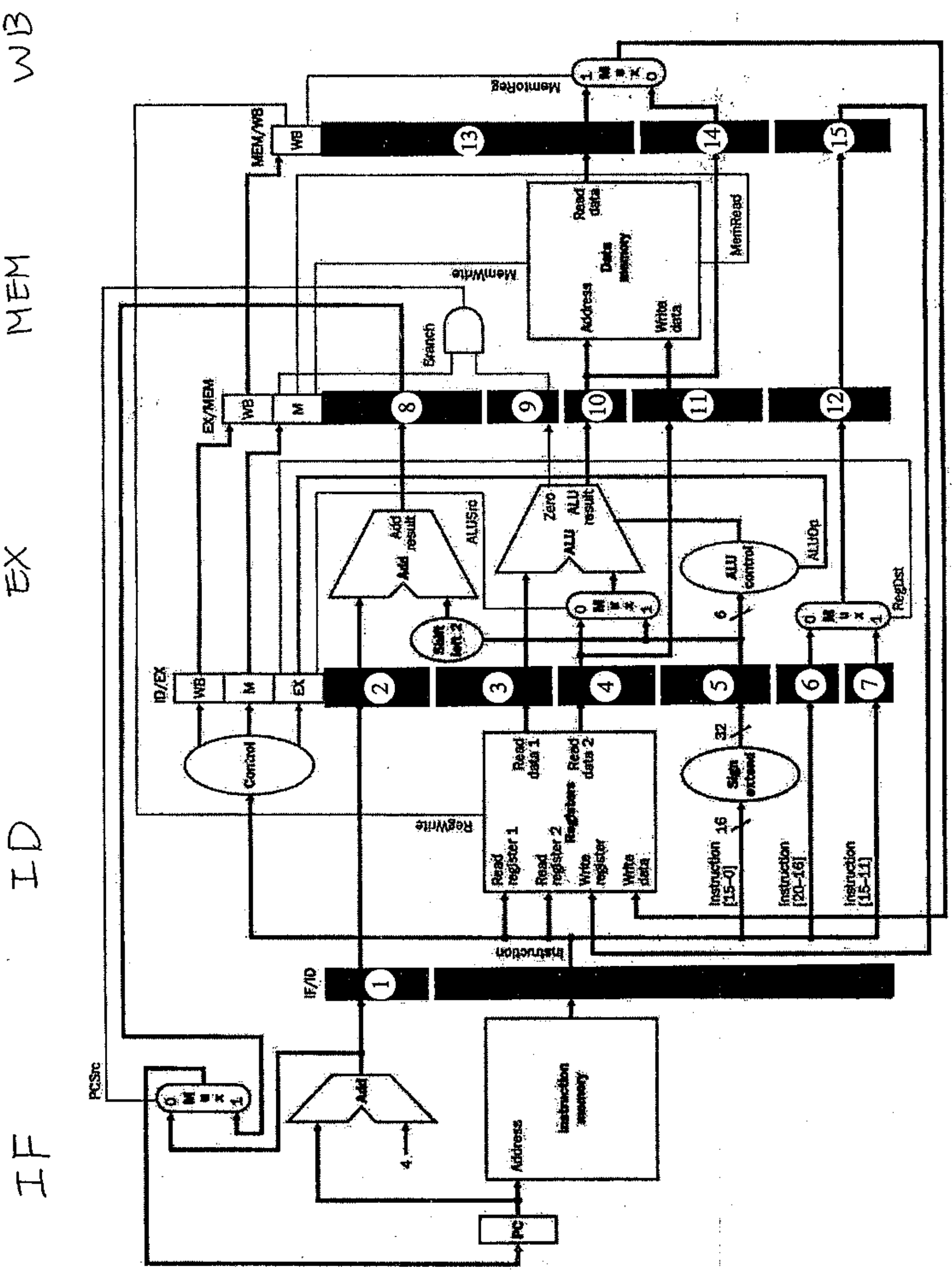
Suppose that the first instruction starts from clock cycle 1. Determine the value of *every* field (1, 2, ..., 15) in the four pipeline registers (IF/ID, ID/EX, EX/MEM, MEM/WB) at the beginning of the clock cycle 5. If you believe a field value is impossible to determine from the information provided, explain why.

Assume that the initial values before the program is executed are as follow:

- PC=500_{ten} which is the address of the lw instruction.
- Every register has the initial value 10_{ten} plus the register number (e.g., register $8 has the initial value 18_{ten}).
- Every memory word accessed as data has the initial value 1000_{ten} plus the byte address of the word (e.g., Mem[8] has the initial value 1008_{ten}).

Fill your answer in the following table and copy it to your answer sheet.

Pipeline Register Field	Value (in decimal number) (Fill your answers in this column.)
1.	
2.	
3.	
4.	
5.	
6.	
7.	
8.	
9.	
10.	
11.	
12.	
13.	
14.	
15.	


IF
ID
EX
MEM
WB
PCSrc
PC
Add
4
Address
Instruction memory
IF/ID
Instruction
RegWrite
Control
Read register 1
Read register 2
Registers
Write register
Write data
Read data 1
Read data 2
Sign extend
16
32
Instruction [15–0]
Instruction [20–16]
Instruction [15–11]
ID/EX
WB
M
EX
Shift left 2
Add result
ALUSrc
Zero
ALU
ALU result
ALU control
ALUOp
6
RegDst
EX/MEM
Branch
MemWrite
Address
Write data
Read data
Data memory
MemRead
MEM/WB
MemtoReg
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

4. (20%) Instruction Set

It is possible to imagine even simpler instruction sets. In this assignment, you are to consider a hypothetical machine called SIC, for Single Instruction Computer. As its name implies, SIC has only one instruction: subtract and branch if negative, or sbn for short. The sbn instruction has three operands, each consisting of the address of a word in memory:

```
sbn a,b,c # Mem[a] = Mem[a] - Mem[b];if (Mem[a]<0) go to c
```

The instruction will subtract the number in memory location b from the number in location a and place the result back in a, overwriting the previous value. If the result is greater than or equal to 0, the computer will take its next instruction from the memory location just after the current instruction. If the result is less than 0, the next instruction is taken from memory location c. SIC has no registers and no instructions other than sbn.

Although it has only one instruction, SIC can imitate many of the operations of more complex instruction sets by using clever sequences of sbn instructions. For example, here is a program to copy a number from location a to location b:

```
start:  sbn temp,temp,.+1   # Sets temp to zero
        sbn temp,a,.+1      # Sets temp to -a
        sbn b,b,.+1         # Sets b to zero
        sbn b,temp,.+1      # Sets b to -temp, which is a
```

In the program above, the notation .+1 means "the address after this one," so that each instruction in this program goes on to the next in sequence whether or not the result is negative. We assume temp to be the address of a spare memory word that can be used for temporary results.

4.1 (10%) Write a SIC program to add a and b, leaving the result in a and leaving b unmodified.

4.2 (10%) Write a SIC program to multiply a by b, putting the result in c. Assume that memory location one contains the number 1. Assume that a and b are greater than 0 and that it's OK to modify a or b. (Hint: What does this program compute?)

```
c = 0; while (b > 0) {b = b - 1; c = c + a;}
```

國立中山大學八十七學年度碩博士班招生考試試題

科 目：作業系統與資料結構(資工所)

1. A five dimensional array A has ranges of dimensions as follows: [-2:7, -4:10, -2:1, -3:2, 1:10]. Assume that the initial address is 38 and each element is 8 bytes. Also assume that array A's entries are counted by a row major order. What is the address of [0, 8, 0, 1, 8]? (10%)
2. Prove that in any graph, the number of vertices of odd degree is even. (10%)
3. We find the number of arithmetic operations for a particular program can be calculated by $T(n) = 4T(n/2) + 1$, where n is the number of loops in the program and $T(1) = 1$. What is the total number of arithmetic operations if there are 4096 loops in the program? (10%)
4. What is time locality and space locality? How can they be used in designing storage systems? (10%)
5. Assume you have a page reference string for a process with m frames (initially all empty). The page reference string has length p with n distinct page numbers occurring in it. For any page-replacement algorithms, a) what is a lower bound on the number of page faults? b) What is an upper bound on the number of page faults? c) When a page fault occurs, describe the actions taken by the operating system? (15%)
6. Prove the following: a) In a tree, any two vertices are connected by a unique path. b) If G is a tree, then $\varepsilon = v - 1$, where ε is the number of edges and v is the number of vertices. (20%)
7. Define concisely: 1) Process. 2) Interprocess communication. 3) Deadlocks. 4) Multiprogramming, and 5) Internal segmentation and external segmentation. (25

1. (20%)A bakery sells eight kinds of bread with different flavors: namely, peanut butter, cream butter, coconut, chocolate, strawberry, cheese, blueberry, and pineapple and their prices are 10, 15, 12, 20, 12, 10, 15, and 25 dollars, respectively. Suppose a customer wants to spend exactly 100 dollars to buy some bread, then
   a) How many choices does he have?
   b) Suppose he wants at least one for bread with the flavors of cream butter, strawberry and cheese, then how many choices does he have?
2. (20%) Let M = (S, I, O, V, W) be a finite state machine where S=$\{s_0, s_1, s_2, s_3, s_4\}$, I={a, b, c}, O={0,1} and V and W are determined by Table 1.

Table 1

	V			W		
	a	b	c	a	b	c
s_0	s_0	s_3	s_2	0	1	1
s_1	s_1	s_2	s_3	0	1	1
s_2	s_1	s_2	s_3	1	1	0
s_3	s_2	s_3	s_0	1	0	1

   a) Starting at s_0, what is the output for input string abbbccc?
   b) Draw the state diagram for this finite state machine.
3. (15%)A student is taking a multiple choice exam in which each question has four possible answers, exactly one of which is correct. If the student knows the answer he selects the correct answer. Otherwise he selects one answer at random from four possible answers. Suppose that the student knows the answer to 75% of the questions.
   a) What is the probability that on a given question the student gets the correct answer?
   b) If the student gets the correct answer to a question, what is the probability that he knows the answer?
   c) Suppose there are twenty problems and each problem is assigned equal weight, i.e. five point for each problem, then what is score he probably gets for the exam.
4. (15%)Let G=(V, E) is a directed graph with |V| = n and |E| = k, the following matrices are used to represent G. Let V = $\{v_1, v_2, \ldots, v_n\}$. Define the adjacency matrix A= $(a_{ij})_{n\times n}$ where a_{ij}=1 if there is a directed edge from v_i to v_j, otherwise a_{ij} = 0. If we calculate A^m using ordinary addition and multiplication, what do the entries in the matrix reveal about G?
5. (10%)Verify whether the following proposition is tautology? (no score without proof)

$$\forall x\{P(x)\rightarrow(\exists y)\{Q(x,y)\}\}\wedge(\forall x)\{\neg P(x)\rightarrow\neg(\exists y)\{Q(x,y)\}\}\Leftrightarrow$$
$$\forall x\{\neg P(x)\vee(\exists y)\{Q(x,y)\}\}\wedge(\forall u)\{P(u)\vee(\forall v)\{\neg Q(u,v)\}\}$$

6. (20%) Determine the sum

$$\binom{n}{0}\binom{m}{k} + \binom{n}{1}\binom{m}{k-1} + \binom{n}{2}\binom{m}{k-2} + \ldots + \binom{n}{k}\binom{m}{0}$$

where $k \le n$ and $k \le m$.