If some questions are unclear or not well defined to you, you can make your own assumptions and state them clearly in the answer sheet.

1. Please choose the most appropriate answer (one only) to each following question. (20%)

1.1 Which of the following MIPS addressing mode means that the operand is a constant within the instruction itself? (a) Register addressing (b) Immediate addressing (c) Base addressing (d) PC-relative addressing

1.2 Which of the following feature is typical for the RISC machine? (a) Powerful instructions (b) Large CPI (c) More addressing modes (d) Poor code density

1.3 Which is the IEEE 754 binary representation for the floating point number -0.4375_{ten} in single precision? (a) 1 11111110 11100000000000000000000 (b) 1 11111110 11000000000000000000000 (c) 1 01111101 11100000000000000000000 (d) 1 01111101 11000000000000000000000

1.4 A program runs in 10 seconds on computer A (which has a 4 GHz clock) and 6 second on computer B. If computer B requires 1.2 times as many clock cycles as computer A for this program. What clock rate does computer B have? (a) 6 GHz (b) 7 GHz (c) 8 GHz (d) 9GHz

1.5 Pipelining improves (a) Instruction throughput (b) Individual instruction execution time (c) Individual instruction latency (d) All of the above are correct

1.6 Which of the following technique is associated primarily with a hardware-based approach to exploiting instruction-level parallelism? (a) Very long instruction word (VLIW) (b) Explicitly parallel instruction computer (EPIC) (c) Dynamic pipeline scheduling (d) Register renaming

1.7 Consider a cache with 64 blocks and a block size of 16 bytes. What block number does byte address 1200 map to? (a) 10 (b) 11 (c) 12 (d) 13

1.8 Which of the following statement about "write back" is incorrect? (a) new value is written only to the block in the cache (b) the modified block is written to the lower level of the hierarchy when it is replaced (c) more complex to implement than write-through (d) can ensure that data is always consistent between cache and memory

1.9 Which of the following statement is incorrect? (a) The compiler must understand the pipeline to achieve the best performance. (b) Deeper pipelining usually increases clock rate. (c) Increasing associativity of cache may slow access time, leading to lower overall performance. (d) The addition of second level cache can reduce miss rate of the first level cache.

1.10 In a magnetic disk, the disks containing the data are constantly rotating. On average it should take half a revolution for the desired data on the disk to spin under the read/write head. Assuming that the disk is rotating at 10,000 revolutions per minute (RPM), what is the average time for the data to rotate under the disk head? (a) 0.1 ms (b) 0.2 ms (c) 3 ms (d) 6 ms

2. Performance Analysis (19%)

2.1 (4%) The following measurements have been made on two different computers: M1 and M2.

Program	Time on M1	Time on M2
1	2.0 seconds	1.5 seconds
2	5.0 seconds	10.0 seconds

Program	Instructions executed on M1	Instructions executed on M2
1	5×10^9	6×10^9

If the clock rates of M1 and M2 are 4 GHz and 6 GHz, respectively, find the clock cycles per instruction (CPI) for program 1 on both computers.

2.2 (4%) Assuming the CPI for program 2 on each computer in Problem 2.1 is the same as the CPI for program 1, find the instruction count for program 2 running on each computer.

2.3 (6%) A compiler designer is trying to decide between two code sequences for a particular computer. The hardware designers have supplied the following facts:

	CPI for this instruction class		
	A	B	C
CPI	1	2	3

For a particular high-level-language statement, the compiler writer is considering two code sequences that require the following instruction counts:

Code sequence	Instruction counts for instruction class		
	A	B	C
1	2	1	2
2	4	1	1

Which code sequence executes the most instructions? Which will be faster? What is the CPI for each sequence?

2.4 (5%) You could speed up a Java program on a new computer by adding hardware support for garbage collection. Garbage collection currently comprises 20% of the cycles of the program. You have two possible changes to the machine. The first one would be to automatically handle garbage collection in hardware. This causes an increase in cycle time by a factor of 1.2. The second would be to provide for new hardware instructions to be added to the ISA that could be used during garbage collection. This would halve the number of instruction needed for garbage collections but increase the cycle time by 1.1. Which of theses two options, if either, should you choose? Why?

3. Datapath and Control (19%)

3.1 (9%) Consider the following machines, and compare their performance using the following instruction frequencies: 25% Loads, 13% Stores, 47% R-type instructions, and 15% Branch/Jump.

M1: The multicycle datapath shown in Fig. 1 with a 1 GHz clock.

M2: A machine like the multicycle datapath of Fig. 1, except that register updates are done in the same clock cycle as a memory read or ALU operation. Thus in Fig. 2 (which shows the complete finite state machine control of Fig. 1), states 6 and 7 and states 3 and 4 are combined. This machine has a 3.2 GHz clock, since the register update increases the length of the critical path.

M3: A machine like M2 except that effective address calculations are done in the same clock cycle as a memory access. Thus states 2, 3, and 4 can be combined, as can 2 and 5, as well as 6 and 7. This machine has a 2.8 GHz clock because of the long cycle created by combining address calculation and memory access.

Find the effective CPI and MIPS (million instructions per second) for all machines.

3.2 (10%) Exception detection is an important aspect of execution handling. Try to identify the cycle in which the following exceptions can be detected for the multicycle datapath in Fig. 1. Consider the following exceptions:

a. Overflow exception

b. Invalid instruction

c. External interrupt

d. Invalid instruction memory address

e. Invalid data memory address

4. Pipelining (28%)

4.1 (6%) Consider the following code segment in C:

```
A = B + E;
C = B + F;
```

Here is the generated MIPS code for this segment, assuming all variables are in memory and are addressable as offsets from $t0:

```
lw    $t1, 0($t0)
lw    $t2, 4($t0)
add   $t3, $t1, $t2
sw    $t3, 12($t0)
lw    $t4, 8($t0)
add   $t5, $t1, $t4
sw    $t5, 16($t0)
```

Find the hazards in the code segment and reorder the instructions to avoid any pipeline stalls.

4.2 (8%) MIPS instructions classically take five steps (IF, ID, EX, MEM WB) to execute in pipeline. To resolving control hazards, the decision about whether to branch in MIPS architecture is moved from MEM stage to the ID stage. Explain the advantage, difficulties, and how to overcome the difficulties when moving the branch execution to the ID stage.

4.3 (8%) Compare the performance for single-cycle, multicycle, and pipelined control by the average instruction time using the following instruction frequencies (25% loads, 10% stores, 11% branches, 2% jumps, and 52% ALU instructions) and functional unit times (200 ps for memory access, 100 ps for ALU operation, and 50 ps for register file read or write). For the multicycle design, the number of clock cycles for each instruction class is shown in Fig. 2. For the pipelined design, loads take 1 clock cycle when there is no load-use dependence and 2 when there is. Branches take 1 when predicted correctly and 2 when not. Jumps always pay 1 full clock cycle of delay, so their average time is 2 clock cycles. Other instructions take 1 clock cycle. For pipelined execution, assume that half of the load instructions are immediately followed by an instruction that uses the result and that one-quarter of the branches are mispridicted. Ignore any other harzards.

4.4. (6%) Suppose the memory access became 2 clock cycles long. Find the relative performance of the single-cycle and multicycle designs by the average instruction time as described in Problem 4.3.

5. Memory Hierarchy (14%)

5.1 (8%) Suppose we have a processor with a base CPI of 1.0, assuming all references hit in the primary cache, and a clock rate of 5 GHz. Assume a main memory access time of 100 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 2%. How much faster will the processor be if we add a secondary cache that has a 5 ns access time for either a hit or a miss and is large enough to reduce the miss rate to main memory to 0.6%?

5.2 (6%) Consider a memory hierarchy using one of the following three organizations for main memory: (a) one-word-wide memory organization, (b) wide memory organization, and (c) interleaved memory organization Assume that the cache block size is 16 words, that the width of organization (b) is four words, and that the number of banks in organization (c) is four. If the main memory latency for a new access is 10 memory bus clock cycles and the transfer time is 1 memory bus clock cycle. Assume that it takes 1 clock cycle to send the address to the main memory, what are the miss penalties for each of these organizations?

國立中山大學９６學年度碩士班招生考試試題

科目：計算機結構【資工系碩士班】

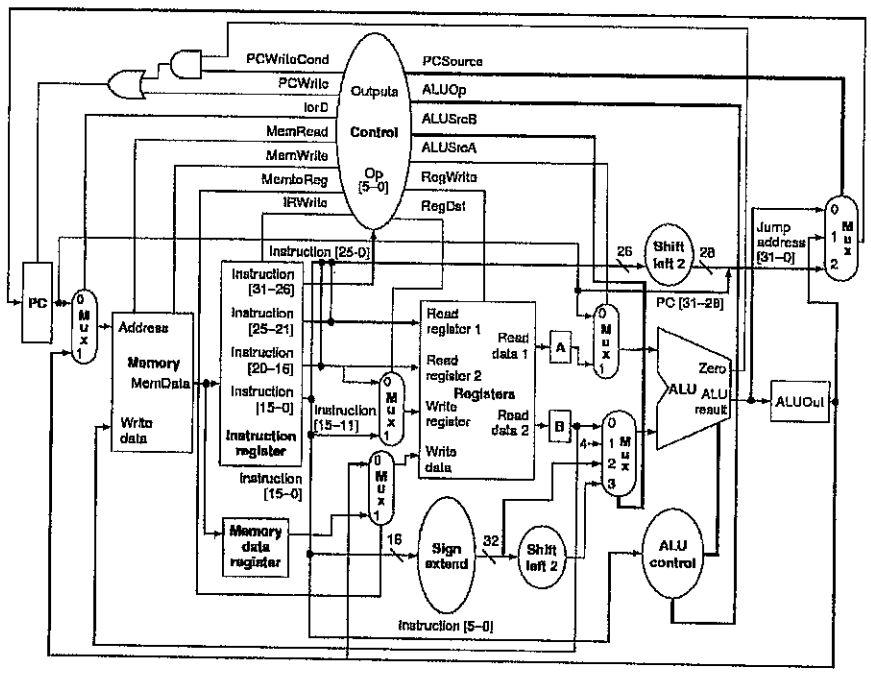


Fig. 1

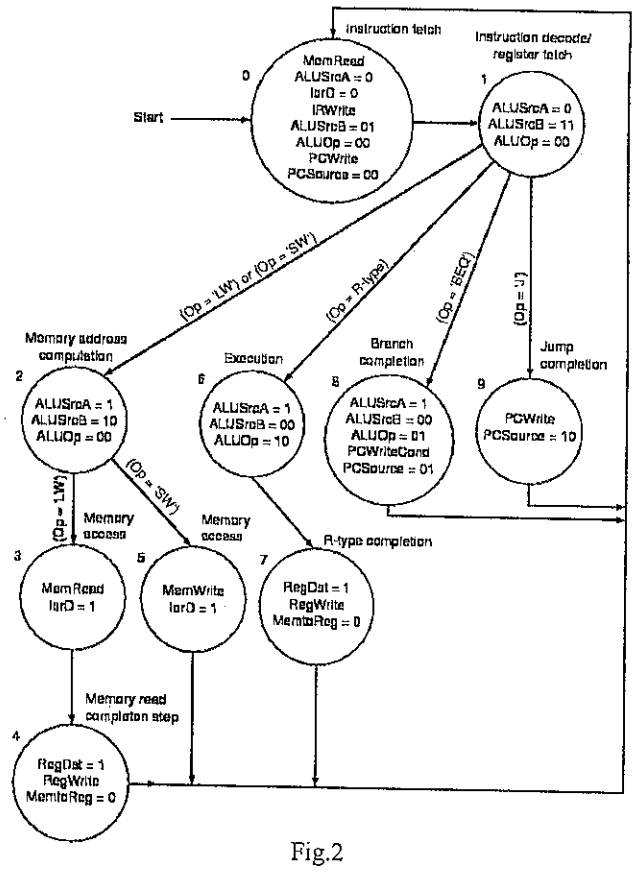


Fig.2

國立中山大學９６學年度碩士班招生考試試題

科目：作業系統與資料結構【資工系碩士班甲組；乙組選考】

1. Consider a paging system with the page table stored in memory.
   (5%) a. If a memory reference takes 100 nanoseconds, how long does a paged memory reference take? Justify your answer.
   (5%) b. If we add associative registers, and 75 percent of all page-table references are found in the associative registers, what is the effective memory reference time? Justify your answer. (Assume that finding a page-table entry in the associative registers takes zero time, if the entry is there.)

2. Suppose that a disk drive has 5000 cylinders, numbered from 0 to 4999. The drive is currently serving a request at cylinder 143, and the previous request was at cylinder 125. The queue of pending requests, in FIFO order, is 86, 1470, 913, 1774, 948, 1509, 1022, 1750, 130.Starting from the current head position, what is the total distance (in cylinders) that the disk arm moves to satisfy all the pending requests, for each of the following disk scheduling algorithms?
   (5%) a. FCFS (First-Come First-Served)
   (5%) b. SSTF (Shortest-Seek-Time-First)
   (5%) c. SCAN
   (5%) d. LOOK

3. (15%) Consider the following program fragments. What are the values that x can take on during the execution of the following threads; assuming x is initialized to 0?

```
Thread 1:{for(i=0;i<10;i++)x=x+2;}
Thread 2:{for(j=0;j<10;j++)x=x-1;}
```

4. Given input 4371, 1323, 6173, 4199, 4344, 9679, 1989 and a hash function $h(x) = x(mod\ 10)$. Show the result:
   (5%) a. Separate chaining hash table.
   (5%) b. Open addressing hash table using linear probing.
   (5%) c. Open addressing hash table using quadratic probing.
   (5%) d. Open addressing hash table with second hash function $h_2(x) = 7-(x\ mod\ 7)$.

5. (15%) For a matrix multiplication problem, e.g., $M_{5*3}M_{3*7}M_{7*2}M_{2*9}M_{9*4}$, please derive the most efficient matrix multiplication method, and also briefly describe your algorithm for the general problem.

6. (10%) a. Insert 5, 1, 10, 2, 8, 4, 9, 6, 7, 3 into an initially empty 2-3 tree. Show your work in sufficient detail.
   (10%) b. Insert 5, 1, 2, 8, 4, 6, 7, 3, 10, 9 into an initially empty AVL tree. Show your work in sufficient detail.

國立中山大學９６學年度碩士班招生考試試題

科目：離散數學【資工系碩士班甲組；乙組選考】

1. Let A be a set with $|A| = n$, and let R be a relation on A that is anti-symmetric.
   (a) [5%] What is the maximum value for $|R|$?
   (b) [5%] How many anti-symmetric relations can have the size?

2. [10%] Let $M = (S, I, O, v, w)$ be a finite state machine, where $S = \{s_1, s_2, s_3, s_4\}$ is the set of states; $I = \{0, 1\}$ is the input alphabet for M; $O = \{0, 1\}$ is the output alphabet for M; $v : S \times I \to S$ is the next state function; and $w : S \times I \to O$ is the output function defined as follows:

	v		w	
	0	1	0	1
s_1	s_4	s_3	0	1
s_2	s_2	s_4	0	0
s_3	s_1	s_2	1	0
s_4	s_1	s_4	1	1

If the starting state for M is not s_1, find an input string x of smallest length such that $v(s_i, x) = s_1$, for all $i = 2, 3, 4$. (Hence, x gets M to s_1 regardless of the starting state.)

3. [10%] Let $n \in Z^+$ with $n \geq 4$. How many subgraphs of the complete graph K_n are isomorphic to the complete bipartite graph $K_{1,3}$?

4. [10%] Alice and Bob toss a loaded coin. The probability of that the result is the head whenever tossing the coin once is p, where $p > 0$. The first to obtain a head is the winner. Alice goes first but, if she tosses a tail, then Bob gets two chances. If he tosses two tails, then Alice again tosses the coin and, if her toss is a tail, then Bob again goes twice (if his first toss is a tail). This continues until someone tosses a head. What value of p makes this a fair game (that is, a game where both Alice and Bob have probability 1/2 of winning)?

5. Let $A = \{x, a, b, c, d\}$
   (a) [5%] How many closed binary operations f on A satisfy $f(a, b) = c$?
   (b) [5%] How many of the functions f in part (a) have an identity ?
   (c) [5%] How many of the functions f in part (b) are commutative ?

6. [15%] A ship carries 48 flags, 12 each of the colors red, white, blue, and black. Twelve of these flags are placed on a vertical pole in order to communicate a signal to other ships. Let N be the number of the signals that contain at least three white flags or no white flags at all. Please use generating functions or exponential generating functions to compute N. In fact, $N = 4^{12} + K \times 3^{11}$ where K is an integer. Find the value of K.

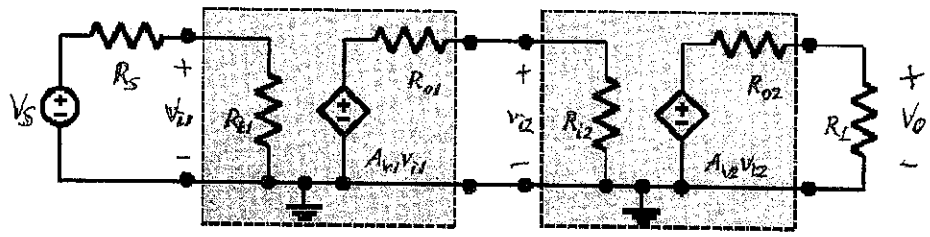
7. [15%] For $n \geq 1$, let a_n be the number of ways to write n as an ordered sum of positive integers, where each summand is at least 2. (For example, $a_5 = 3$ because here we may represent 5 by 5, by 2 + 3, and by 3 + 2.) Find and solve a recurrence relation for a_n. (Please explain your answer.)

8. [15%] Let $p = 61$, $q = 127$, and $n = pq = 7747$. Find the smallest positive integer d such that $((1234^{17})^d \bmod n) = 1234$. Please explain how to obtain your answer.

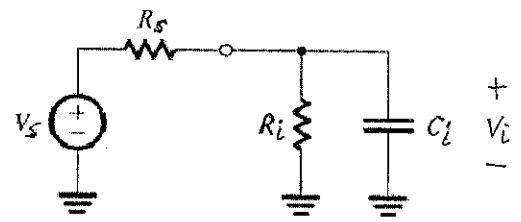
國立中山大學９６學年度碩士班招生考試試題

科目：電子學【資工系碩士班乙組選考】

1. (10%) Find the voltage gain of the following circuit?

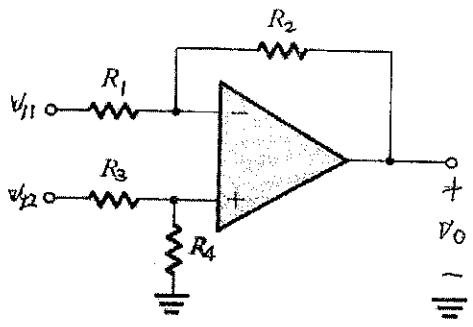


2. (10%) Derive an expression for $V_i(s)/V_s(s)$.



3. (15%) What are the definitions of V_{OL}, V_{OH}, V_{IL}, V_{IH}, NM_L, NM_H? (2.5% of each definition)

4. (15%) Consider the difference amplifier in the following picture with two input terminals connected together to an input common-mode signal source. For $R_2/R_1 = R_4/R_3$, show that the input common-mode resistance is $(R_3 + R_4) \| (R_1 + R_2)$.



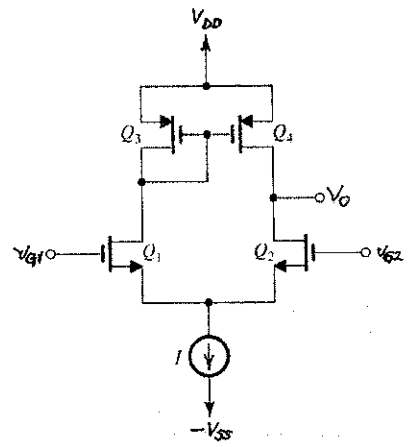
5. (20%) (a) (10%) What is the highest frequency if a triangle wave of 10-V peak-to-peak amplitude that can be reproduced by an op amp whose slew rate is 20 V/μs? (b) (10%) For a sine wave of the same frequency, what is the maximum amplitude of the output signal that remains undistorted?

國立中山大學９６學年度碩士班招生考試試題

科目：電子學【資工系碩士班乙組選考】

6. (15%) The circuit in the following figure provides a constant current I_O as long as the circuit to which the collector is connected maintains the BJT in the active mode. Show that $I_O = \alpha \dfrac{V_{CC}[R_2/(R_1+R_2)] - V_{BE}}{R_E + (R_1 \| R_2)/(\beta+1)}$

7. (15%) In the following circuit, all transistors have $k'W/L$=3.2mA/V^2, and $|V_A|$=20V. Find the bias current I for which the gain v_o/v_{id} =80V/V.



(a)

國立中山大學９６學年度碩士班招生考試試題

科目：工程數學【資工系碩士班乙組選考】

Problem 1. (Totally, 10 points) Mathematically prove that $\sum_{n=1}^{\infty} n^{-2} < 3$.

Problem 2. (Totally, 10 points) Let C be the set of all complex numbers. Let $S_1 = \{z|z \in C, |z| \leq 1\}$ and $S_2 = \{z|z \in C, Re(z) \geq 0.5\}$. Let $S = S_1 \cap S_2$. Draw a figure to show the set S in the Gauss (complex) plane and calculate the area of S.

Problem 3. (Totally, 30 points)

Let μ, A, B be given positive real numbers.

(1). (10 points) Suppose $P(x)$ is a function defined in the interval $[-B, A]$. Solve the following differential equation:

$$\mu \cdot P^{'}(x) + 0.5 \cdot P^{''}(x) = 0, P(A) = 1, P(-B) = 0 \tag{1}$$

(2). (10 points) Show that $P(x)$ is an increasing function of x in the interval $[-B, A]$ and $P(x) \in [0, 1], \forall x \in [-B, A]$.

(3). (10 points) Suppose $A = B$. Let X be a random variable that is uniformly distributed in the interval $[-A, A]$. Let $Y \in \{0, 1\}$ be a binary random variable. In addition, $P\{Y = 1|X = x\} = P(x)$, $\forall x \in [-A, A]$. Calculate $E[Y]$, the expected value of the random variable Y.

Problem 4. (Totally, 30 points)

$$A = \begin{bmatrix} 2 & -1 & 0 \\ -1 & 2 & -1 \\ 0 & -1 & 2 \end{bmatrix}$$

(1). (10 points) Calculate the determinant of the matrix A and the eigenvalues of the matrix A.

(2). (10 points) Prove that the matrix A is positive-definite.

(3). (10 points) Diagonalize the matrix A such that $A = Q \times D \times Q^{-1}$, where D is a diagonal matrix. Derive the values of the matrix D and the matrix Q.

Problem 5. (Totally, 20 points)

Let $v_1 = (1, 0, 0)$, $v_2 = (-1, 1, 1)$, and $v_3 = (0, 4, 2)$ be three vectors.

(1). (10 points) Prove that $\beta = \{v_1, v_2, v_3\}$ is a basis for the three-dimensional Euclidean space R^3.

(2). (10 points) Let $x = (x_1, x_2, x_3)$ be a vector and $x = c_1 \cdot v_1 + c_2 \cdot v_2 + c_3 \cdot v_3$. Derive the values of c_1, c_2, and c_3 in terms of x_1, x_2, and x_3.