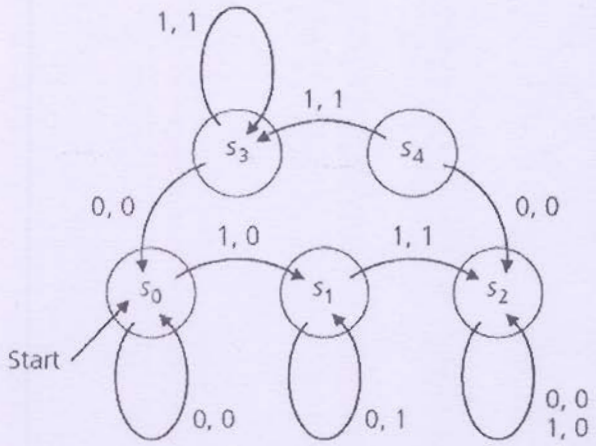
1. [10%] An executive buys \$2490 worth of presents for the children of her employees. For each girl she gets an art kit costing \$33; each boy receives a set of tools costing \$29. How many presents of each type did she buy? Note that all of your answers should be in the format of integers, not formulae.

2. A finite state machine M has input alphabet $I = \{0, 1\}$ and output alphabet $O = \{0, 1\}$, and is determined by the state diagram shown in the following figure.
   (a) [5%] Determine the output string for the input string 110111, starting at s_0. What is the last transition state?
   (b) [5%] In which state should we start so that the input string 10010 produces the output 10000?
   (c) [5%] Let s_4 be the starting state. Determine an input string $x \in I^*$ of minimal length such that the last transition state is s_1. Is x unique?



3. [10%] Let $\Sigma = \{a, b, c\}$. Determine the smallest number of words one must select from Σ^4 to guarantee that at least two of the words start and end with the same letter.

4. (a) [5%] Let $A = \{1, 2, 3, 4, 5\} \times \{1, 2, 3, 4, 5\}$ and define R on A by $(x_1, y_1)\ R\ (x_2, y_2)$ if $x_1 + y_1 = x_2 + y_2$. Determine the equivalence class $[(4, 3)]$.
   (b) [5%] If $A = \{1, 2, 3, 4, 5, 6, 7\}$, define R on A by $(x, y) \in R$ if $x - y$ is a multiple of 3. Determine the partition of A induced by R.

5. (a) [10%] Ten students enter a locker room that contains 10 lockers. The first student opens all the lockers. The second student changes the status (from closed to open, or vice versa) of every other locker, starting with the second locker. The third student then changes the status of every third locker, starting at the third locker. In general, for $1 < k \leq 10$, the kth student changes the status of every kth locker, starting with the kth locker. After the tenth student has gone through the lockers, which lockers are left open?
(b) [5%] Answer part (a) if 10 is replaced by $n \in \mathbf{Z}^+$, $n \geq 2$.

6. [10%] Find the coefficient of x^{15} in $\dfrac{x^3 - 5x}{(1-x)^3}$. Note that the format of your answer should be an integer.

7. [10%] The general solution of the recurrence relation $a_{n+2} + b_1 a_{n+1} + b_2 a_n = b_3 n + b_4$, $n \geq 0$, with b_i constant for $1 \leq i \leq 4$, is $c_1 2^n + c_2 3^n + n - 7$. Find b_i for each $1 \leq i \leq 4$.

8. [10%] How many subgraphs does K_6 have? (If two subgraphs are isomorphic but have different vertex sets, consider them distinct.) Note that the format of your answer should be an integer.

9. (a) [5%] Find all the elements of order 10 in $(Z_{40}, +)$.
(b) [5%] Let $G = \langle a \rangle$ be a cyclic group of order 40. Which elements of G have order 10?

I. 單選題：(18%, 2% per question)

1.1 Which one of the following descriptions about RISC computers is NOT correct?
(a) The cycle time is usually reduced.
(b) ALU instructions can access memory.
(c) The instruction format is uniform.
(d) None of above.

1.2 Which of the following is NOT a register-transfer level component (RTL)?
(a) register, (b) adder, (c) AND gate (d) decoder.

1.3 How many memory accesses are required to execute a "store" instruction with memory indirect addressing?
(a) 0 (b) 1 (c) 2 (d) 3.

1.4 Which one about the microprogrammed control is correct?
(a) They are located in the datapath part of a CPU.
(b) The microprogram is stored in main memory.
(c) It is easier to design microprogrammed control than hardwired control.
(d) Microprogrammed control is faster than hardwired control.

1.5 Which architecture is classified as instruction-level parallel processing?
(a) super scalar, (b) massive parallel processing (MPP), (c) symmetrical parallel processing (SMP), (d) vector processor.

1.6 Processor performance can be improved by all the following techniques except
(a) reducing clock cycle time,
(b) executing multiple instructions concurrently,
(c) increasing the number of pipeline stages,
(d) using powerful instructions.

1.7 Interrupt signals cannot be generated by
(a) NOP instruction, (b) page faults, (c) arithmetic exceptions, (d) I/O device requests.

1.8 Which one of the following systems may contain a microprocessor?
(a) personal computer, (b) digital HDTV, (c) mobile phone, (d) all of above.

1.9 An I/O device whose maximum bandwidth is 100,000 bits/sec is connected to a computer system. The I/O controller interrupts the CPU whenever it receives a byte. The interrupt handling routine consists of 100 instructions. The CPU executes 10 million instructions per second on the average. What percentage of the CPU's time is used to serve the I/O device, assuming that the device transmits data with the maximum speed?
(a) 1.25%, (b) 2.5% (c) 12.5%, (d) 25%.

II. (12%, 3% per question) Briefly answer the following questions.

2.1 What is the virtual memory system?

2.2 Modern computers only allow load/store instructions to access memory. Please explain the advantage of this approach.

2.3 What is the hardwired control?

2.4 When you perform addition on two n-bit numbers with 2's complement representation, how do you determine whether there is overflow? Let the two words be $A=a_{n-1}\ldots a_1a_0$ and $B=b_{n-1}\ldots b_1b_0$.

III. (24%) Basic logic design

3.1 $X(=x_1x_0)$ and $Y(=y_1y_0)$ are both unsigned 2-bit binary numbers, and assume that X is always larger than Y. In this problem, we will design a logic circuit to calculate the difference $Z(=z_1z_0)$; in other words, $Z = X - Y$.

(a) (5%) Draw the K-maps of z_1 and z_0. (Hint: Both z_1 and z_0 are functions of x_1, x_0, y_1 and y_0.)

(b) (5%) Give minimum sum-of-product (SOP) realization of z_1 and z_0.

3.2 Determine the logic function of the sequential circuit shown in Fig. 1, which is implemented with T Filp-Flops.

(a) (4%) Complete the state transition table shown in Table 1. In this Table, Q_A^+ and Q_B^+ specify the logic values stored in Q_A and Q_B fter a clock is applied. T_A and T_B are the inputs of the T Filp-Flops, as shown in Fig. 1.

(b) (4%) Draw the complete state transition diagram. What is the function of this circuit?

(c) (6%) Assume that only D Filp-Flops are available (i.e., you can't use T Filp-Flops). Redesign the circuit with D Filp-Flops. In the combinational part of your design, use AND, OR, and Inverter gates only.

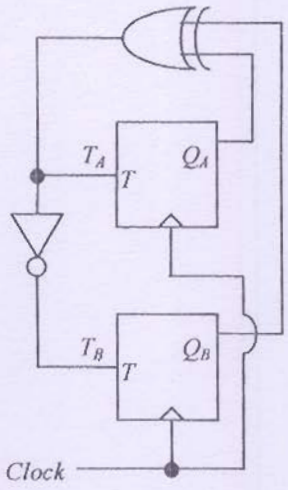


Fig. 1

Table 1

Q_A	Q_B	T_A	T_B	Q_A^+	Q_B^+
0	0				
0	1				
1	0				
1	1				

IV. (12%) Performance Analysis

4.1 (8%) The following results are measured for the same source code that is performed in two different processors:

Measurement	Processor A	Processor B
Instruction count	5 billion	4 billion
Clock rate	500 MHz	500 MHz
CPI	1	1.2

(a) (4%) Which processor has the higher MIPS (million instructions per second) rating?

(b) (4%) Which processor is faster?

4.2 (4%) In a modified version of Processor B, a new instruction I_X is invented to replace instructions I_Y and I_Z whenever I_Y and I_Z appear in sequence. However, this modification reduces clock rate to 450 MHz, while the CPI is not affected. Assume that in the program given in Problem 4.1, there are 200 million I_Y instructions followed by I_Z. What is the execution time if the program is executed in the new processor? Does the modification improve performance?

V. (12%) A computer uses a direct-mapped cache with 16 KB of data and 4-word blocks.

5.1 (6%) What is the size of the tag field, assuming 32-bit address? What is the total size of the cache?

5.2 (6%) Assume address 003C5A64 (in hexadecimal) is generated by the computer. Which block in the cache should be searched, and how to decide if the data is in cache?

VI. (22%) Datapath design.

6.1 (4%) In a multicycle implementation of the MIPS instruction set, the number of clock cycles required to execute instruction classes are given as follows:

Loads	Stores	ALU	Branches	Jumps
5	4	4	3	3

Assume that the instruction mix for a given program is 25% loads, 10% stores, 11% branches, 2% jumps, and 52% ALU. What is the CPI of this program?

6.2 In a pipelined implementation of the MIPS instruction set, the datapath is divided into 5 stages: instruction fetch (IF), instruction decode and register file read (ID), execution or address calculation (EX), data memory access (MEM), and write back (WB). The clock cycle time of this machine is the same as the one in Problem 6.1.

(a) (2%) Assume that there are no pipeline hazards, what is the CPI of this machine?

(b) (2%) Compared to the multicycle implementation given in Problem 6.1, how much faster this pipelined datapath is if there are no hazards?

(c) (2%) How do you handle the hazards, if no hardware solutions are available?

6.3 The following MIPS code will be executed in the machine described in Problem 6.2.

```
sub  $2,   $1,  $3
and  $11,  $2,  $5
or   $12,  $6,  $2
add  $13,  $2,  $2
sw   $14,  100($2)
```

(a) (4%) List all possible data hazards.

(b) (2%) Whenever a data hazard is detected, the instruction pipeline has to be stalled. How many cycles are required to execute the above codes?

(c) (6%) In order to reduce stall cycles due to data hazards, a pipeline structure with forwarding unit is provided as shown in Fig. 2. Describe how data hazards in the above code are resolved in this structure.

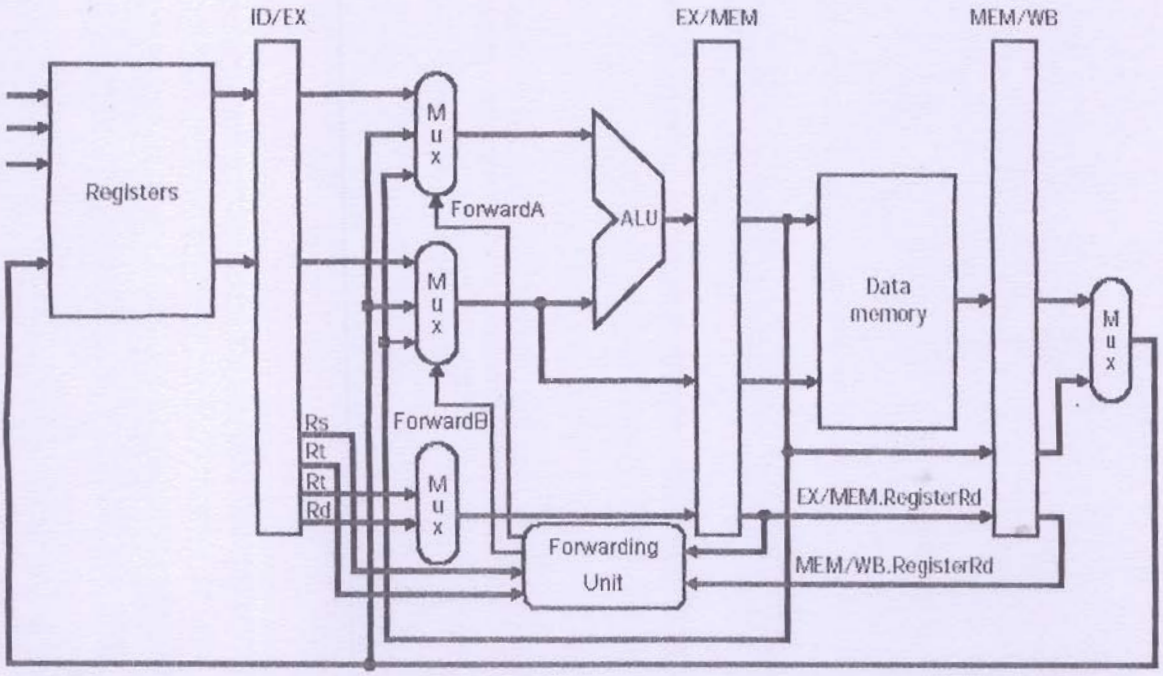


Fig. 2

INSTRUCTIONS: *If any question is unclear or you believe some assumptions need to be made, state your assumptions clearly at the beginning of your answer.*

1. (20%) Consider the following program that uses the Pthreads API. What would be the output of the program? (*Note that the line numbers are for references only.*)

```
1  #include <stdio.h>
2  #include <stdlib.h>
3  #include <unistd.h>
4  #include <pthread.h>
5  #include <sys/types.h>
6
7  int value = 1;
8
9  static void *runner(void *param);
10
11 int main(int argc, char **argv)
12 {
13     pid_t pid = fork();
14     if (pid > 0) {
15         printf("A = %d\n", value);
16     }
17     else if (pid == 0) {
18         pid_t pid = fork();
19         if (pid > 0) {
20             printf("B = %d\n", value);
21         }
22         else if (pid == 0) {
23             pid_t pid = fork();
24             pthread_t tid;
25             pthread_attr_t attr;
26             pthread_attr_init(&attr);
27             pthread_create(&tid, &attr, runner, NULL);
28             pthread_join(tid, NULL);
29             if (pid > 0)
30                 printf("C = %d\n", value);
31             else
32                 printf("D = %d\n", value);
33         }
34         else {
35             exit(1);
36         }
37     }
38     else {
39         exit(1);
40     }
41 }
42
43 static void *runner(void *param)
44 {
45     value += 1;
46     pthread_exit(0);
47 }
```

2. A computer has four page frames. The time of loading, time of last access, and the R and M bits for each page are as shown below (the times are in clock ticks):

Page	Loaded	Last Reference	R	M
0	126	279	0	0
1	230	260	1	0
2	120	272	1	1
3	160	280	1	1

   (a) (5%) Which page will NRU replace?

   (b) (5%) Which page will FIFO replace?

   (c) (5%) Which page will LRU replace?

   (d) (5%) Which page will second chance replace?

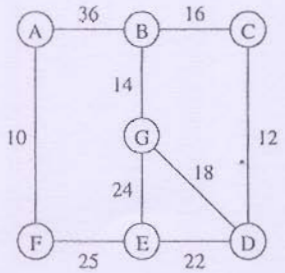
3. Consider the following preemptive priority-scheduling algorithm based on dynamically changing priorities. Larger priority numbers imply higher priority. When a process is waiting for the CPU (in the ready queue but not running), its priority changes at a rate α; when it is running, its priority changes at a rate β. All processes are given a priority of 0 when they enter the ready queue. The parameters α and β can be set to give many different scheduling algorithms.

   (a) (5%) What is the algorithm that results from $\alpha < \beta < 0$? (**Just give the name of the algorithm.**)

   (b) (5%) What is the algorithm that results from $\beta > \alpha > 0$? (**Just give the name of the algorithm.**)

4. (15%) Analyze the behavior of QUICKSORT in the case where a schizophrenic adversary picks the best possible splitter (partitioning element) instead of the worst, every other time (i.e., he alternates between best and worst). What running time is induced by this "adversary?"

5. Consider the following weighted graph.



   (a) (10%) Show the order in which the edges are added to the minimum cost spanning tree using Prim's algorithm. (**Use weight to represent edges in your answer and just show the order.**)

   (b) (10%) Show the order in which the edges are added to the minimum cost spanning tree using Kruskal's algorithm. (**Use weight to represent edges in your answer and just show the order.**)

6. (15%) When we traverse a binary tree, we find that the tree in preorder is $ABDCEGFHI$, in inorder is $DBAGECHFI$, and in postorder is $DBAGECHIF$. Draw the tree.

1. **(28 %)** The relative areas of the transistors in the amplifier circuit shown in Fig. 1 are all unity except for Q3 which has a relative area of 2. Assume $V_T \cong 25mV$, $\beta = 200$ and $V_{BEQ} \cong 0.6V$ for all transistors.

   (a) Calculate the dc current of each transistor. (8%)

   (b) Calculate the small signal voltage gain of this circuit. (10%)

   (c) Find out the dc output voltage assuming Vin=0. If this dc output voltage is not zero, discuss how to modify the circuit to achieve zero dc output. (5%)

   (d) Discuss the problem if the CMRR of this differential amplifier is not good. By matching the two sides of the differential input perfectly, the CMRR can be improved. Propose one different approach which can lead to better CMRR. (5%)

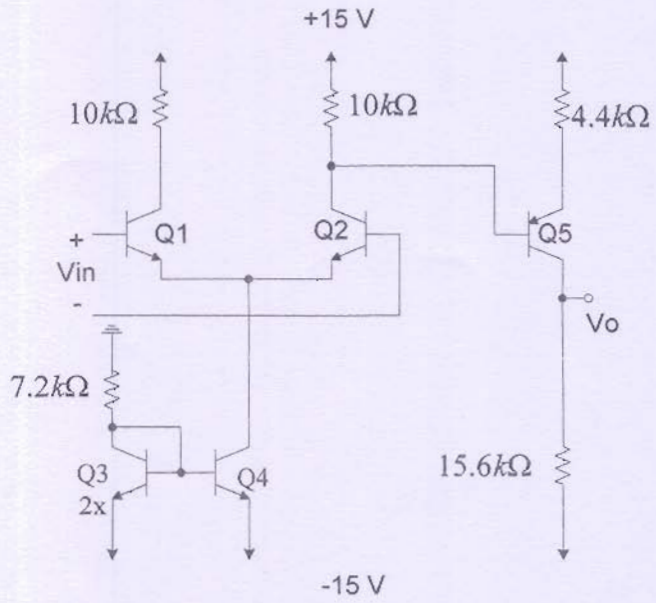


Fig. 1

2. **(20 %)** For the circuit shown in Fig.2 , we assume $r_o = \infty$, $k_n \frac{W}{L} = 0.25\,mA/V^2$, $V_t = 2V$ and $C_1 = C_2 = 1uF$.

   (a) Find out the midband voltage gain and the input resistance R_{in}. (12%)

   (b) Find out the low-frequence 3-dB frequency. (8 %)

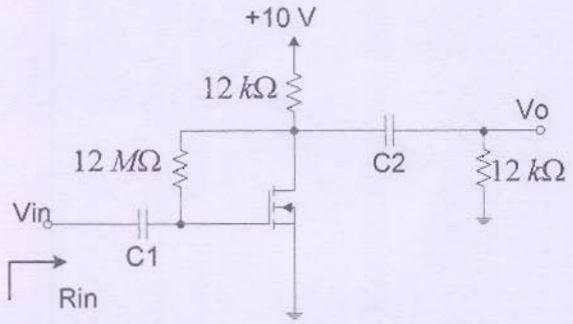


Fig. 2

3. **(22 %)** Answer the following questions regarding the OP-AMP circuit,.

(a) Design an OP-AMP circuit which can compute the output voltage $V_{out} = 2V_1 - 4V_2$ where V_1 and V_2 represent two input voltages. (10%)

(b) Determine the output voltage if the input $(d_1 d_2 \cdots d_8)$ to an ideal 8-bit DAC as shown in Fig.3 is 10100001. The reference voltage V_{ref} equals 3V. (6%)

(c) Discuss how to use R_3 to cancel the effect of bias for the circuit shown in Fig. 4, and determine the value of R_3. (6%)

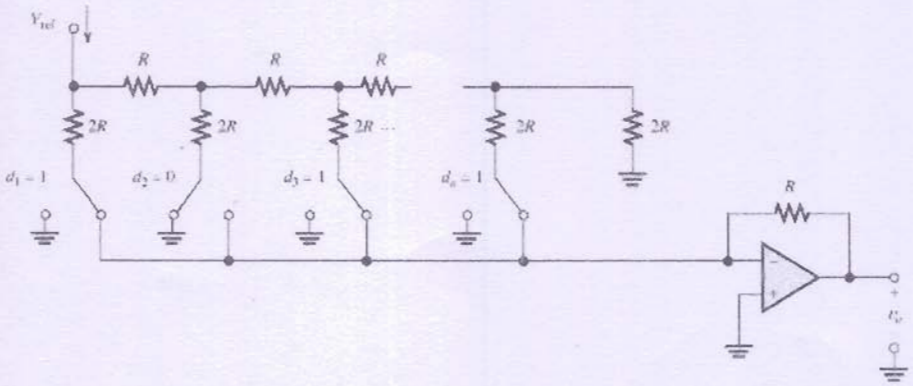


Fig. 3

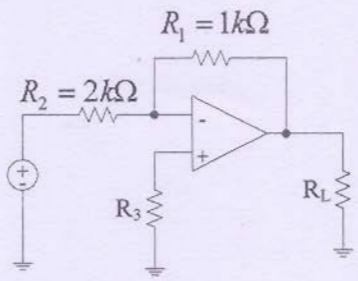


Fig. 4

4. **(30 %)** Answer the following questions regarding the digital logic circuit:

(a) Consider a resistor-pull-up NMOS inverter shown in Fig. 5, what effect (an increase, a decrease or none) will increasing R_D have on (a) t_{PHL} (b) t_{PLH} (c) V_{OH} (d) V_{OL} (e) static power dissipation (10 %)

(b) Consider the following CMOS inverter as shown in Fig.6. The parameter for N-MOS and P-MOS is $V_{tn} = |V_{tp}| = 3V$ and $k_n \frac{w}{L} = k_p \frac{w}{L} = 0.25\, mA/V^2$, find out the instantaneous maximum power dissipated during the period when the input is switching from 0 to 5V. (6 %)

(c) Draw a circuit diagram of a 4-input CMOS gate that realizes the logic function $Y = \overline{(A+B)CD}$. (7%)

(d) For your CMOS circuit design for (c), specify W/L ratios for all transistors in terms of the ratios ***n*** and ***p*** of the basic inverter, such that the worst-cast t_{PHL} and t_{PLH} of the gate are equal to those of the basic inverter. (7%)

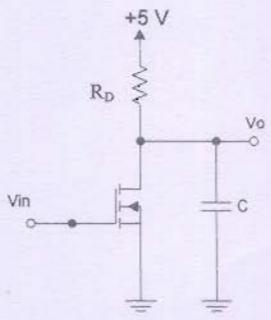


Fig. 5

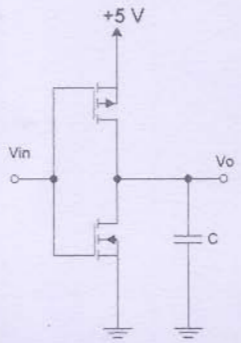


Fig. 6

總分 100 分，請依序作答。

1. **(20%)** Given a continuous-time signal x(t). The Fourier Transform of x(t) can be denoted as X(jω).

   (a). (8%) Find the inverse Fourier transform for the following signals:

   a. $X(j\omega) = 2 + 2\cos(\omega)$

   b. $X(j\omega) = \dfrac{5}{(3 + j\omega)^2}$

   (b). (12%) Find the Fourier Transforms of the following signals:

   a. $x(t) = u(t + \frac{1}{2}T) - u(t - \frac{1}{2}T)$

   b. $x(t) = e^{-t}u(t) - e^{-t}u(t-4)$

   c. $x(t) = \sin(4\pi t)\sin(50\pi t)$

2. **(18%) Systems.**

   Consider the following three systems:

   System A : $y(t) = x(t+2)\sin(\omega t + 2)$, *where* $\omega \neq 0$

   System B : $y[n] = \left(-\dfrac{1}{2}\right)^n (x[n] + 1)$

   System C : $y[n] = \sum_{k=1}^{n} (x^2[k+1] - x[k])$

   Where x and y are the input and the output of each system.

   For each of the system, please state whether or not the system is (i) linear; (ii) time-invariant; (iii) causal. Provide either a brief justification or an example to prove your answer.

3. **(15%)** Suppose that the frequency response of a continuous-time LTI system is :

$$H(j\omega) = \frac{4 - \omega^2}{1 + j\omega}$$

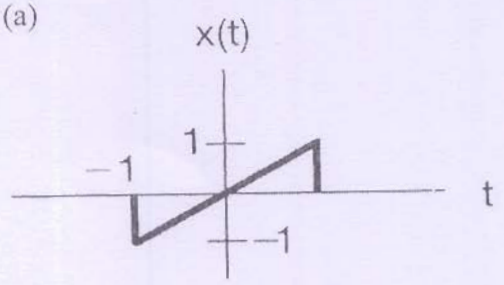
   and the input is :

$$x(t) = 4\cos(t) + \cos(2t)$$

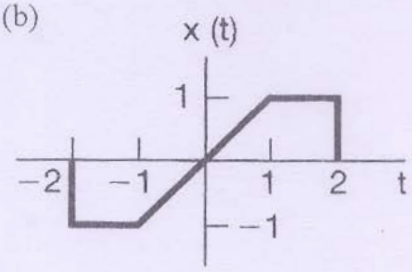
   Determine the output y(t) of the system.

4. **(16%)** Calculate the Fourier Transform $X(j\omega)$ of each of the following signals, x(t):

(a)



(b)



5. **(16%) Convolution.**

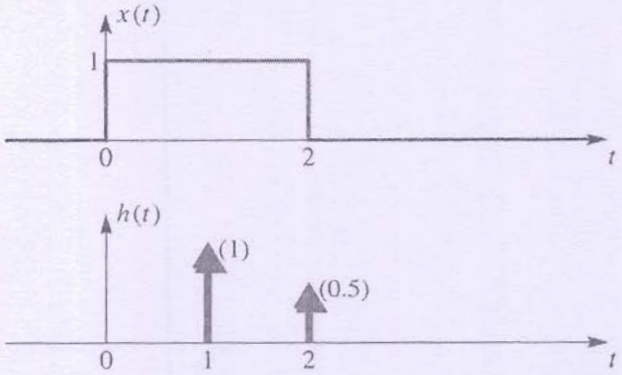
(a). (3%) Determine the convolution of two discrete-time impulse signals:

$$\delta[n-n_1]*\delta[n-n_2].$$

(b). (5%) Use the result of (a) to determine the convolution of the following two discrete-time signals:

$$x[n]=\delta[n+2]+\delta[n-6]$$
$$h[n]=\delta[n+3]+\delta[n]$$

(c). (8%) calculate the convolution of the following two signals, x(t) and h(t):



plot the result of x(t)*h(t) as a function of t in details.

6. **(15%)** Suppose that an LTI system has system function equal to:

$$H(z)=1-3z^{-2}+2z^{-3}+4z^{-6}$$

(a). (5%) determine the difference equation that relates the output y[n] of the system to the input x[n].

(b). (5%) determine and plot the impulse response h[n]

(c). (5%) use z-transforms and polynomial multiplication to find the sequence $y[n] = x[n]*h[n]$ when the input to the system is the sequence: $x[n]=2\delta[n]+\delta[n-1]-2\delta[n-2]+4\delta[n-4]$.